PATENT ABSTRACTS OF JAPAN

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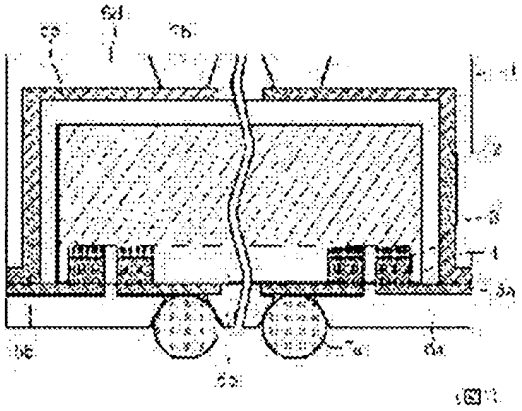
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To achieve the high-density packaging of a semiconductor device, and to improve the use efficiency of the area of a chip by preventing the design of the semiconductor device from being restricted, and by preventing the area of the semiconductor chip from being increased even if an external terminal is provided on both the upper and lower surfaces of the semiconductor device.



SOLUTION: On the surface of the active element of the semiconductor chip 2, an electrode 3 made of Al is formed, and is connected to a conductor 5a via a bump 4. One portion of the conductor 5a is connected to a soldering ball as an external terminal 7a, and the other is connected to a conductor 5b extended from the side to upper surface (back surface) of the chip. The partial region of the conductor 5b is set to an external terminal 7b. An insulator 6b is filled between the semiconductor chip 2 and conductor 5b, the side and upper surface of the semiconductor chip are covered with an insulator 6c, and the entire semiconductor 1 other than an external terminal formation region is covered with insulators 6a and 6d.

LEGAL STATUS

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JAPANESE [JP,2002-093942,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

* NOTICES *

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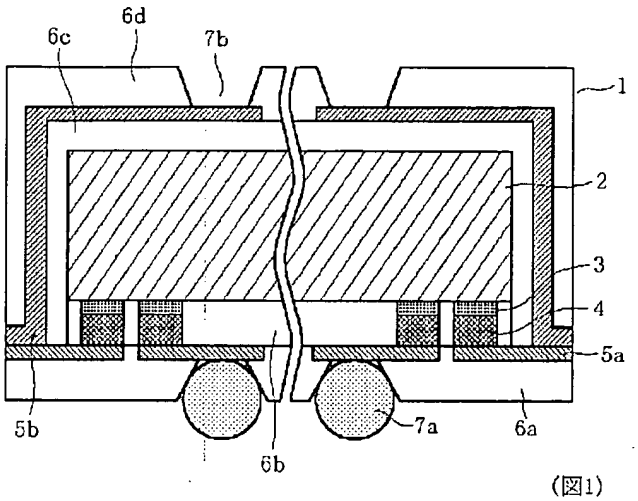
CLAIMS

[Claim(s)]
[Claim 1] The rewiring layer which includes wiring which stands in a row in the metal electrode of a semiconductor chip in the 1st principal plane of a semiconductor chip is formed. In the semiconductor device with which the 1st external terminal is formed on said rewiring layer on said 1st principal plane, and the 2nd external terminal connected to said rewiring layer is formed on the 2nd principal plane which is the field of the opposite side of said 1st principal plane It is the semiconductor device characterized by connecting the 2nd external terminal with said rewiring layer through side-face wiring formed in the side face of a chip, and bending the 1st principal plane side edge section of said side-face wiring in the shape of an "L" character, and the bent part touching the field by the side of the 2nd [of said rewiring layer / said] principal plane.
[Claim 2] It is the semiconductor device according to claim 1 characterized by constituting at least one side with the conductive ball among the said 1st and 2nd external terminal.
[Claim 3] Some [at least] external terminals are semiconductor devices according to claim 1 or 2 characterized by being constituted by the wiring part from which the wrap insulator layer was alternatively removed in the wiring layer top.
[Claim 4] The semiconductor device according to claim 1 characterized by forming the external terminal also in said side-face wiring.
[Claim 5] It is the semiconductor device according to claim 1 characterized by connecting the end of some rewiring layers to the 1st external terminal, and connecting the other end with the 2nd external terminal through said side-face wiring.
[Claim 6] The semiconductor device characterized by forming in the side face of said semiconductor chip side-face wiring connected to said a part of rewiring layer in the semiconductor device with which the rewiring layer which includes wiring which stands in a row in the metal electrode of a semiconductor chip in the 1st principal plane of a semiconductor chip is formed, and the 1st external terminal is formed on said rewiring layer on said 1st principal plane, and forming the external terminal in this side-face wiring.
[Claim 7] (1) The process which cuts so that the rear face of said rewiring layer may expose the wafer with which the rewiring layer including wiring which stands in a row in a metal electrode is formed on the 1st principal plane, and forms a slot, (2) (3) With the process which embeds an insulator in the slot formed of cutting The process which forms the through hole to which the rear face of said rewiring layer is exposed in the predetermined part of the embedded insulator, (4) An end the internal surface of said through hole connected to said rewiring layer Wrap side-face wiring, the process in which an end forms the 2nd principal plane wiring layer which was connected to said side-face wiring, and which extends on the 2nd [of a wafer] principal plane, and (5) -- the manufacture approach of the semiconductor device characterized by having the process which cuts along with the cutting plane line in the process of said ** (1), and is carved into each chip.
[Claim 8] The manufacture approach of the semiconductor device according to claim 7 characterized by adding the process which forms the insulator which covers said 2nd principal plane wiring top except an

external terminal formation field top in advance of the process of said ** (5) after the process of said ** (4), and is filled up with the inside of said through hole.
[Claim 9] The manufacture approach of the semiconductor device according to claim 7 characterized by cutting of the process of said ** (1) being performed by the dicer.
[Claim 10] The manufacture approach of the semiconductor device according to claim 7 characterized by carrying out opening of the through hole using a laser beam in the process of said ** (3).
[Claim 11] In the process of said ** (4) The manufacture approach of the semiconductor device according to claim 7 characterized by forming a wiring layer by plating.

[Translation done.]

Drawing selection Representative drawing



(図1)

1 半導体装置
2 半導体チップ
3 電極
4 バンプ
5a、5b 導体
6a、6b、6c、6d 絶縁体
7a、7b 外部端子

[Translation done.]

JAPANESE [JP,2002-093942,A]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which has an external terminal to vertical both sides of a semiconductor chip, and its manufacture approach in more detail about a semiconductor device and its manufacture approach.
[0002]
[Description of the Prior Art] In recent years, the demand to the miniaturization of an electronic instrument or a system and improvement in the speed is increasing much more, and in order to respond to this, in respect of mounting technology, importance has been attached to the wafer level CSP technique of performing packaging in a wafer phase from CSP (chip size package). Three-dimension mounting technology which carries out the laminating of the chip and enables higher-density mounting with this is being realized. In order to realize such three-dimension mounting, it is necessary to prepare an external terminal in front flesh-side both sides of a chip.
[0003] Drawing 6 is the sectional view of the conventional semiconductor device 21 (henceforth the 1st conventional example) which has an external terminal to front flesh-side both sides of a chip produced by the wafer level CSP technique. As shown in drawing 6 , the electrode 23 which consists of aluminum etc. is formed in the active element side of a semiconductor chip 22, and the chip front face is covered with insulator 26b except for the bump formation field top. the conductor with which some electrodes 23 were formed on insulator 26b through the bump 24 -- it connects with 25a. an insulator 26b top and a conductor -- 25a top is covered with insulator 26a except for the external terminal formation field. the field in which insulator 26a is not formed -- a conductor -- 25a is exposed and external terminal 27a has fixed there. the conductor formed in the chip rear face through the beer plug 20 formed by some electrodes 23 penetrating a substrate -- it connects with 25b. a semiconductor chip top and a conductor -- 25b top is covered with insulator 26c except for the field used as external terminal 27b. However, in this 1st conventional example, since it was necessary to carry out opening of the through hole to a semiconductor chip 22 in order to form a beer plug, and the opening location of that through hole received component arrangement and a leading-about limit of wiring, constraint might be received in the design of a semiconductor device. Moreover, there was also a trouble that the surface integral of a through hole and semiconductor chip area will become large.
[0004] On the other hand, the technique which connects wiring formed in the chip table and the rear face through the electric conduction film (connection) formed in the tip side side is proposed by JP,2000-91496,A. Drawing 7 is the sectional view of the semiconductor device (henceforth the 2nd conventional example) indicated in this official report. As shown in this drawing, the wiring 32 and 33 formed in the top face of the silicon substrate 31 of CSP30 is connected to the pillar-shaped electrode 36 through the wiring 35 formed in the inferior surface of tongue of the connection 34 formed in the side face of a silicon substrate 31, and a silicon substrate 31. And CSP30 is carried through the different direction electroconductive glue 38 on the wiring substrate 37, and a bare chip 39 is carried on CSP30.
[0005]

[Problem(s) to be Solved by the Invention] The 1st conventional example mentioned above had the trouble that a chip area will increase, when the degree of freedom of a design received constraint and a chip area was consumed by the through hole. On the other hand, in the 2nd conventional example, since the contact section of the connection 34 and wiring 35 which connect a chip table and a rear face is limited only to the side face of wiring 35, there is a fault to which connection becomes unstable or contact resistance becomes high. while the technical problem of this invention is solving the trouble of the conventional technique mentioned above, and the purpose enables it to connect between a chip table and a rear face, without [without it restrains the degree of freedom of a design, and] increasing a chip area -- between a chip table and a rear face -- low resistance -- and dependability -- it is enabling it to connect highly.

[0006]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, according to this invention, the rewiring layer which includes wiring which stands in a row in a metal electrode in the 1st principal plane of a semiconductor chip is formed. In the semiconductor device with which the 1st external terminal is formed on said rewiring layer on said 1st principal plane, and the 2nd external terminal connected to said rewiring layer is formed on the 2nd principal plane which is the field of the opposite side of said 1st principal plane The 2nd external terminal is connected with said rewiring layer through side-face wiring formed in the side face of a chip, and the 1st principal plane side edge section of said side-face wiring is bent in the shape of an "L" character, and semiconductor device ** to which the bent part is characterized by being in contact with the rear face of said rewiring layer is offered.

[0007] moreover -- according to [in order to attain the above-mentioned purpose] this invention -- (1) -- with the process which cuts so that the rear face of said rewiring layer may expose the wafer with which the rewiring layer including wiring which stands in a row in a metal electrode is formed on the 1st principal plane, and forms a slot (2) (3) With the process which embeds an insulator in the slot formed of cutting The process which forms the through hole to which the rear face of said rewiring layer is exposed in the predetermined part of the embedded insulator, (4) An end the internal surface of said through hole connected to said rewiring layer Wrap side-face wiring, The process in which an end forms the 2nd principal plane wiring layer which was connected to said side-face wiring, and which extends on the 2nd [of a wafer] principal plane, (5) Manufacture approach ** of the semiconductor device characterized by having the process which cuts along with the cutting plane line in the process of said ** (1), and is carved into each chip is offered.

[0008] And the process which forms the insulator which covers said 2nd principal plane wiring top except an external terminal formation field top in advance of the process of said ** (5) after the process of said ** (4), and is preferably filled up with the inside of said through hole is added. Moreover, cutting of the process of said ** (1) is preferably performed by the dicer. Furthermore, in the process of said ** (3), opening of the through hole is preferably carried out using a laser beam. Moreover, in the process of said ** (4), a wiring layer is formed by plating much more preferably.

[0009]

[Embodiment of the Invention] Next, with reference to a drawing, it is based on an example and the gestalt of operation of this invention is explained. Drawing 1 is the sectional view of the semiconductor device 1 of the 1st example of this invention. A dimension is 10x10xt0.3mm, using silicon in a semiconductor chip 2. And on the active element side (inferior surface of tongue) of a semiconductor chip 2, 300 electrodes 3 made from aluminum are arranged along the circumference of a chip with the dimension of 0.1x0.1mm. an electrode 3 -- a bump 4 -- minding -- a conductor -- it connects with 5a electrically. some conductors -- the conductor with which external terminal 7a fixes to the point of 5a, and some [other] conductors are prolonged from a tip side side to a chip top face -- it connects with 5b. Some fields which are conductor 5b are external terminal 7b.

[0010] a bump 4 -- Au, conductor 5a, and a conductor -- 5b was formed using Cu. a bump's 4 thickness -- 50 micrometers, conductor 5a, and a conductor -- the thickness of 5b could be 20 micrometers. Although the PbSn (lead and tin) solder of 250 micrometers of diameters of a ball was used for external terminal 7a, the insulating ball with which the conductive film was formed in other solder and front

faces may be used. Moreover, nothing may not be like external terminal 7b. moreover, a semiconductor chip 2 and a conductor -- between 5a, the passivation film and insulator 6b to which illustration was abbreviated and which have opening on an electrode 3 are formed. The side face and top face of a semiconductor chip are covered with insulator 6c, and the semiconductor device 1 whole is covered with the insulators 6a and 6d which have opening on an external terminal formation field. Insulators 6a and 6d is [the thickness on the top face of a chip of 50 micrometer thickness and insulator 6c] 20 micrometers in an epoxy resin at a solder resist. Moreover, insulator 6b is formed with low elastic resin, such as polyimide. Although the inside 6a and 6d of these insulators is not necessarily required, forming on dependability is desirable.

[0011] The descriptions of the semiconductor device of this invention are to have an electrode to vertical both sides of a semiconductor device, to have wiring for it on a semiconductor chip side face, and that connection with the side-face wiring (conductor 5b) and rewiring layer (conductor 5a) is attained by contact on a flat surface. Thus, when a side face has wiring with which electrical installation is attained by superficial contact, a semiconductor chip can be designed, without being restrained as usual, without spoiling the dependability of electric connection. Furthermore, any number of steps of this semiconductor device can be easily piled up by forming a solder ball in external terminal 7a like this example, and connecting with external terminal 7b of other semiconductor devices.

[0012] Drawing 2 - drawing 4 are the sectional views showing the manufacture approach of the 1st example of this invention in order of a process. First, on the wafer 8 covered with insulator 6e which has the electrode 3 made from aluminum and has opening on an electrode 3, and which is the passivation film, Ti/TiN which serves as barrier metal by the spatter is deposited, Au is deposited on it and plating substrate layer 4a is formed [drawing 2 (a)]. Next, the plating resist film 12 which has opening of the same pattern as the passivation film on a semi-conductor wafer (insulator 6e) is formed by the photolithography method [drawing 2 (b)]. Next, about 50 micrometers of Au(s) are deposited with electrolysis plating, a bump 4 is formed, and exfoliation removal of the plating resist film 12 is carried out after that [drawing 2 (c)].

[0013] Next, etching removal of the unnecessary plating substrate layer 3a is carried out by using the bump 4 as a mask, and insulator 6b is deposited all over after that. In addition, suppose that plating substrate layer 4a is included and shown to a bump 4, and insulator 6e is included in insulator 6b, and it is shown in subsequent displays [drawing 2 (d)]. Next, flattening is ground and carried out until a bump's 4 front face exposes the insulator 6b by the CMP method. After forming the plating resist film 13 on it furthermore, plating activation is performed, a catalyst bed is formed in the whole surface, and only the catalyst bed on the plating resist film 13 is removed. and an electroless deposition method -- Cu -- 20 micrometers -- depositing -- a conductor -- 5a is formed. The rewiring layer 11 is formed of the above [drawing 2 (e)]. Next, exfoliation removal of the plating resist film 13 is carried out, 50 micrometers of solder resists are deposited all over the, insulator 6a is formed, and patterning of the resist mask 14 is carried out on it [drawing 2 (f)].

[0014] Next, dry etching removes insulator 6a on an external electrode formation field by using the resist mask 14 as a mask [drawing 3 (g)]. In addition, it may be made to perform the process of etching of this insulator 6a in the case of the process of next drawing 4 (l). Next, a slot 9 is formed in order to cut this to a semiconductor chip 2. the cutting depth -- the conductor of the rewiring layer 11 -- it carried out to to this side of 5a, and the place whose insulator 6b is lost completely. The condition was set to the blade thickness of 300 micrometers, the cutting speed of 60mm/second, and rotational frequency 30000rpm at cutting using dicing equipment. Moreover, infrared radiation was used for positioning of cutting of the direction of a flat surface at this time. Since infrared radiation had the property which penetrates silicon, it carried out the image processing of the aluminum recognition mark on the front face of a semiconductor chip (not shown), read it, and was positioned.

[0015] the depth of cutting -- perfect -- insulator 6b -- losing -- and a conductor -- it is necessary to control 5a in the depth to leave Wear of the mechanical precision of the depth direction of dicing equipment and a blade and member thickness dispersion are thought as an error of the depth direction. The mechanical precision of equipment is 0.5 micrometers. Moreover, if the wear of some lines of a

blade is cut and offset will be applied on the way, it is cancellable. cutting dispersion in member thickness -- a conductor -- what is necessary is to take into consideration only thickness dispersion of insulator 6a which is below it, since it is to this side of 5a Since it is only one layer of insulator 6this time, it is stopped by about 2 micrometers. Therefore, it is about total 2.5micrometer, and since grinding of the five ais only deeply carried out about 2.5 micrometers of conductors even if it cuts by expecting this, it is satisfactory. performing grinding, when a rewiring layer turns into a multilayer **** -- a conductor -- [drawing 3 (h)] which needs the device of thickening thickness of 5a.

[0016] Next, skiing JINGU of the epoxy resin of optimum dose was applied and carried out on the wafer 8 cut top face, it embedded in the slot 9, and insulator 6c was formed in the wafer top face and the slot 9. And 150-degree-C heat treatment of 1 hour is performed, and insulator 6c is stiffened [drawing 3 (i)]. Next, a through hole 10 is formed in the predetermined part of embedded insulator 6c. Laser was used for this through hole formation. a through hole 10 -- insulator 6c -- forming -- a conductor -- although 5a must not be penetrated, since it is possible to delete by the laser output with the weaker insulator in an insulator and a conductor -- [drawing 3 (j)] with an easy setup of laser radiation conditions.

[0017] next, the plating substrate layer which consists of Ti/TiN and Cu by the spatter -- forming -- a conductor -- the electrolytic plating after forming the plating resist film which has opening on a formation field -- Cu -- depositing -- a through hole 10 wall, base, and insulator 6c top -- a conductor -- 5b is formed. thereby -- an electrode 3, a bump 4, conductor 5a, and a conductor -- 5b is connected electrically. Next, the plating resist film is removed and etching removal of the exposed plating substrate layer is carried out [drawing 4 (k)]. 6d of next, insulators which are a solder resist -- forming -- alternative -- opening -- carrying out -- a conductor -- [drawing 4 (l)] which exposes 5b and forms external terminal 7b. Then, external terminal 7a is formed. Other solder may be used although the PbSn (lead and tin) solder of 250 micrometers of diameters of a ball was used for external terminal 7a. Moreover, nothing may not be like external terminal 7b [drawing 4 (m)]. . At the end, it cuts and a semiconductor device 1 is obtained. Dicing equipment was used for cutting. Dicing conditions were set to the blade thickness of 50 micrometers, the cutting speed of 60mm/second, and rotational frequency 30000rpm [drawing 4 (n)].

[0018] Drawing 5 is the sectional view of the semiconductor device 1 of the 2nd example of this invention. the same reference number should give a part equivalent to the part of the example shown in drawing 1 in drawing 5 -- the explanation which overlaps in that of ********** is omitted. this example -- setting -- the conductor of the side face of a semiconductor device 1 -- external electrode 7c is prepared in 5b. Thereby, the further high density assembly becomes possible. Moreover, the manufacture approach of this semiconductor device 1 is the same as the manufacture approach of the semiconductor device 1 of drawing 1 , and after the cutting process shown in drawing 4 (n) is completed, it is acquired by laser's etc. removing 6d of some insulators, and preparing external electrode 7c.

[0019] As stated above, the description of the manufacture approach of the semiconductor device of this invention is that it can carry out wafer batch processing in spite of [drawing 3 (h)] cut once, in order to form wiring of a side face, after performing rewiring in the state of a wafer. Since the rewiring layer is supporting the semiconductor chip even if it cuts a wafer, positioning at each process is easy. Moreover, a man day can also be reduced for batch processing.

[0020] As mentioned above, although the desirable example of this invention was explained, proper modification is possible for this invention within limits which are not limited to these examples and do not deviate from the summary of this invention. For example, although a bump's formation approach was performed with electrolysis plating, you may form with the bonding method, vacuum deposition, or a replica method. moreover, the conductor same in the example -- although the external terminals 7b and 7c were formed on 5b, you may make it not form other external terminals in conductor 5b in which external terminal 7c was formed Moreover, in the example, all external terminals may prepare the external terminal mutually connected by Conductors 5a and 5b, without connecting with an electrode if needed, although it connects with the electrode 3 of a semiconductor chip.

[0021]

[Effect of the Invention] As explained above, the semiconductor device of this invention can secure the degree of freedom of a design of a semiconductor chip, without spoiling the dependability of electric connection, since an external terminal is arranged on vertical both sides of a semiconductor device and superficial contact realizes a connection with the rewiring layer of side-face wiring for it while aiming at a deployment of a chip area. Moreover, formation and the external terminal of wiring of a tip side side can be formed by wafer batch processing, and the handling at the time of manufacture becomes easy, maintaining a wafer condition, even if it cut the wafer, since the wafer was cut without cutting a rewiring layer, and positioning at each process also becomes easy, and, as a result, the manufacture approach of the semiconductor device of this invention can aim at reduction of a manufacture man day.

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TECHNICAL FIELD

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PRIOR ART

[Description of the Prior Art] In recent years, the demand to the miniaturization of an electronic instrument or a system and improvement in the speed is increasing much more, and in order to respond to this, in respect of mounting technology, importance has been attached to the wafer level CSP technique of performing packaging in a wafer phase from CSP (chip size package). Three-dimension mounting technology which carries out the laminating of the chip and enables higher-density mounting with this is being realized. In order to realize such three-dimension mounting, it is necessary to prepare an external terminal in front flesh-side both sides of a chip.
[0003] Drawing 6 is the sectional view of the conventional semiconductor device 21 (henceforth the 1st conventional example) which has an external terminal to front flesh-side both sides of a chip produced by the wafer level CSP technique. As shown in drawing 6 , the electrode 23 which consists of aluminum etc. is formed in the active element side of a semiconductor chip 22, and the chip front face is covered with insulator 26b except for the bump formation field top. the conductor with which some electrodes 23 were formed on insulator 26b through the bump 24 -- it connects with 25a. an insulator 26b top and a conductor -- 25a top is covered with insulator 26a except for the external terminal formation field. the field in which insulator 26a is not formed -- a conductor -- 25a is exposed and external terminal 27a has fixed there. the conductor formed in the chip rear face through the beer plug 20 formed by some electrodes 23 penetrating a substrate -- it connects with 25b. a semiconductor chip top and a conductor -- 25b top is covered with insulator 26c except for the field used as external terminal 27b. However, in this 1st conventional example, since it was necessary to carry out opening of the through hole to a semiconductor chip 22 in order to form a beer plug, and the opening location of that through hole received component arrangement and a leading-about limit of wiring, constraint might be received in the design of a semiconductor device. Moreover, there was also a trouble that the surface integral of a through hole and semiconductor chip area will become large.
[0004] On the other hand, the technique which connects wiring formed in the chip table and the rear face through the electric conduction film (connection) formed in the tip side side is proposed by JP,2000-91496,A. Drawing 7 is the sectional view of the semiconductor device (henceforth the 2nd conventional example) indicated in this official report. As shown in this drawing, the wiring 32 and 33 formed in the top face of the silicon substrate 31 of CSP30 is connected to the pillar-shaped electrode 36 through the wiring 35 formed in the inferior surface of tongue of the connection 34 formed in the side face of a silicon substrate 31, and a silicon substrate 31. And CSP30 is carried through the different direction electroconductive glue 38 on the wiring substrate 37, and a bare chip 39 is carried on CSP30.

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, the semiconductor device of this invention can secure the degree of freedom of a design of a semiconductor chip, without spoiling the dependability of electric connection, since an external terminal is arranged on vertical both sides of a semiconductor device and superficial contact realizes a connection with the rewiring layer of side-face wiring for it while aiming at a deployment of a chip area. Moreover, formation and the external terminal of wiring of a tip side side can be formed by wafer batch processing, and the handling at the time of manufacture becomes easy, maintaining a wafer condition, even if it cut the wafer, since the wafer was cut without cutting a rewiring layer, and positioning at each process also becomes easy, and, as a result, the manufacture approach of the semiconductor device of this invention can aim at reduction of a manufacture man day.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The 1st conventional example mentioned above had the trouble that a chip area will increase, when the degree of freedom of a design received constraint and a chip area was consumed by the through hole. On the other hand, in the 2nd conventional example, since the contact section of the connection 34 and wiring 35 which connect a chip table and a rear face is limited only to the side face of wiring 35, there is a fault to which connection becomes unstable or contact resistance becomes high. while the technical problem of this invention is solving the trouble of the conventional technique mentioned above, and the purpose enables it to connect between a chip table and a rear face, without [without it restrains the degree of freedom of a design, and] increasing a chip area -- between a chip table and a rear face -- low resistance -- and dependability -- it is enabling it to connect highly.

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MEANS

[Means for Solving the Problem] In order to attain the above-mentioned purpose, according to this invention, the rewiring layer which includes wiring which stands in a row in a metal electrode in the 1st principal plane of a semiconductor chip is formed. In the semiconductor device with which the 1st external terminal is formed on said rewiring layer on said 1st principal plane, and the 2nd external terminal connected to said rewiring layer is formed on the 2nd principal plane which is the field of the opposite side of said 1st principal plane The 2nd external terminal is connected with said rewiring layer through side-face wiring formed in the side face of a chip, and the 1st principal plane side edge section of said side-face wiring is bent in the shape of an "L" character, and semiconductor device ** to which the bent part is characterized by being in contact with the rear face of said rewiring layer is offered.
[0007] moreover -- according to [in order to attain the above-mentioned purpose] this invention -- (1) -- with the process which cuts so that the rear face of said rewiring layer may expose the wafer with which the rewiring layer including wiring which stands in a row in a metal electrode is formed on the 1st principal plane, and forms a slot (2) (3) With the process which embeds an insulator in the slot formed of cutting The process which forms the through hole to which the rear face of said rewiring layer is exposed in the predetermined part of the embedded insulator, (4) An end the internal surface of said through hole connected to said rewiring layer Wrap side-face wiring, The process in which an end forms the 2nd principal plane wiring layer which was connected to said side-face wiring, and which extends on the 2nd [of a wafer] principal plane, (5) Manufacture approach ** of the semiconductor device characterized by having the process which cuts along with the cutting plane line in the process of said ** (1), and is carved into each chip is offered.
[0008] And the process which forms the insulator which covers said 2nd principal plane wiring top except an external terminal formation field top in advance of the process of said ** (5) after the process of said ** (4), and is preferably filled up with the inside of said through hole is added. Moreover, cutting of the process of said ** (1) is preferably performed by the dicer. Furthermore, in the process of said ** (3), opening of the through hole is preferably carried out using a laser beam. Moreover, in the process of said ** (4), a wiring layer is formed by plating much more preferably.
[0009]
[Embodiment of the Invention] Next, with reference to a drawing, it is based on an example and the gestalt of operation of this invention is explained. Drawing 1 is the sectional view of the semiconductor device 1 of the 1st example of this invention. A dimension is 10x10xt0.3mm, using silicon in a semiconductor chip 2. And on the active element side (inferior surface of tongue) of a semiconductor chip 2, 300 electrodes 3 made from aluminum are arranged along the circumference of a chip with the dimension of 0.1x0.1mm. an electrode 3 -- a bump 4 -- minding -- a conductor -- it connects with 5a electrically. some conductors -- the conductor with which external terminal 7a fixes to the point of 5a, and some [other] conductors are prolonged from a tip side side to a chip top face -- it connects with 5b. Some fields which are conductor 5b are external terminal 7b.
[0010] a bump 4 -- Au, conductor 5a, and a conductor -- 5b was formed using Cu. a bump's 4 thickness -- 50 micrometers, conductor 5a, and a conductor -- the thickness of 5b could be 20 micrometers.

Although the PbSn (lead and tin) solder of 250 micrometers of diameters of a ball was used for external terminal 7a, the insulating ball with which the conductive film was formed in other solder and front faces may be used. Moreover, nothing may not be like external terminal 7b. moreover, a semiconductor chip 2 and a conductor -- between 5a, the passivation film and insulator 6b to which illustration was abbreviated and which have opening on an electrode 3 are formed. The side face and top face of a semiconductor chip are covered with insulator 6c, and the semiconductor device 1 whole is covered with the insulators 6a and 6d which have opening on an external terminal formation field. Insulators 6a and 6d is [the thickness on the top face of a chip of 50 micrometer thickness and insulator 6c] 20 micrometers in an epoxy resin at a solder resist. Moreover, insulator 6b is formed with low elastic resin, such as polyimide. Although the inside 6a and 6d of these insulators is not necessarily required, forming on dependability is desirable.

[0011] The descriptions of the semiconductor device of this invention are to have an electrode to vertical both sides of a semiconductor device, to have wiring for it on a semiconductor chip side face, and that connection with the side-face wiring (conductor 5b) and rewiring layer (conductor 5a) is attained by contact on a flat surface. Thus, when a side face has wiring with which electrical installation is attained by superficial contact, a semiconductor chip can be designed, without being restrained as usual, without spoiling the dependability of electric connection. Furthermore, any number of steps of this semiconductor device can be easily piled up by forming a solder ball in external terminal 7a like this example, and connecting with external terminal 7b of other semiconductor devices.

[0012] Drawing 2 - drawing 4 are the sectional views showing the manufacture approach of the 1st example of this invention in order of a process. First, on the wafer 8 covered with insulator 6e which has the electrode 3 made from aluminum and has opening on an electrode 3, and which is the passivation film, Ti/TiN which serves as barrier metal by the spatter is deposited, Au is deposited on it and plating substrate layer 4a is formed [drawing 2 (a)]. Next, the plating resist film 12 which has opening of the same pattern as the passivation film on a semi-conductor wafer (insulator 6e) is formed by the photolithography method [drawing 2 (b)]. Next, about 50 micrometers of Au(s) are deposited with electrolysis plating, a bump 4 is formed, and exfoliation removal of the plating resist film 12 is carried out after that [drawing 2 (c)].

[0013] Next, etching removal of the unnecessary plating substrate layer 3a is carried out by using the bump 4 as a mask, and insulator 6b is deposited all over after that. In addition, suppose that plating substrate layer 4a is included and shown to a bump 4, and insulator 6e is included in insulator 6b, and it is shown in subsequent displays [drawing 2 (d)]. Next, flattening is ground and carried out until a bump's 4 front face exposes the insulator 6b by the CMP method. After forming the plating resist film 13 on it furthermore, plating activation is performed, a catalyst bed is formed in the whole surface, and only the catalyst bed on the plating resist film 13 is removed. and an electroless deposition method -- Cu -- 20 micrometers -- depositing -- a conductor -- 5a is formed. The rewiring layer 11 is formed of the above [drawing 2 (e)]. Next, exfoliation removal of the plating resist film 13 is carried out, 50 micrometers of solder resists are deposited all over the, insulator 6a is formed, and patterning of the resist mask 14 is carried out on it [drawing 2 (f)].

[0014] Next, dry etching removes insulator 6a on an external electrode formation field by using the resist mask 14 as a mask [drawing 3 (g)]. In addition, it may be made to perform the process of etching of this insulator 6a in the case of the process of next drawing 4 (l). Next, a slot 9 is formed in order to cut this to a semiconductor chip 2. the cutting depth -- the conductor of the rewiring layer 11 -- it carried out to to this side of 5a, and the place whose insulator 6b is lost completely. The condition was set to the blade thickness of 300 micrometers, the cutting speed of 60mm/second, and rotational frequency 30000rpm at cutting using dicing equipment. Moreover, infrared radiation was used for positioning of cutting of the direction of a flat surface at this time. Since infrared radiation had the property which penetrates silicon, it carried out the image processing of the aluminum recognition mark on the front face of a semiconductor chip (not shown), read it, and was positioned.

[0015] the depth of cutting -- perfect -- insulator 6b -- losing -- and a conductor -- it is necessary to control 5a in the depth to leave Wear of the mechanical precision of the depth direction of dicing

equipment and a blade and member thickness dispersion are thought as an error of the depth direction. The mechanical precision of equipment is 0.5 micrometers. Moreover, if the wear of some lines of a blade is cut and offset will be applied on the way, it is cancellable. cutting dispersion in member thickness -- a conductor -- what is necessary is to take into consideration only thickness dispersion of insulator 6a which is below it, since it is to this side of 5a Since it is only one layer of insulator 6this time, it is stopped by about 2 micrometers. Therefore, it is about total 2.5micrometer, and since grinding of the five ais only deeply carried out about 2.5 micrometers of conductors even if it cuts by expecting this, it is satisfactory. performing grinding, when a rewiring layer turns into a multilayer **** -- a conductor -- [drawing 3 (h)] which needs the device of thickening thickness of 5a.

[0016] Next, skiing JINGU of the epoxy resin of optimum dose was applied and carried out on the wafer 8 cut top face, it embedded in the slot 9, and insulator 6c was formed in the wafer top face and the slot 9. And 150-degree-C heat treatment of 1 hour is performed, and insulator 6c is stiffened [drawing 3 (i)]. Next, a through hole 10 is formed in the predetermined part of embedded insulator 6c. Laser was used for this through hole formation. a through hole 10 -- insulator 6c -- forming -- a conductor -- although 5a must not be penetrated, since it is possible to delete by the laser output with the weaker insulator in an insulator and a conductor -- [drawing 3 (j)] with an easy setup of laser radiation conditions.

[0017] next, the plating substrate layer which consists of Ti/TiN and Cu by the spatter -- forming -- a conductor -- the electrolytic plating after forming the plating resist film which has opening on a formation field -- Cu -- depositing -- a through hole 10 wall, base, and insulator 6c top -- a conductor -- 5b is formed. thereby -- an electrode 3, a bump 4, conductor 5a, and a conductor -- 5b is connected electrically. Next, the plating resist film is removed and etching removal of the exposed plating substrate layer is carried out [drawing 4 (k)]. 6d of next, insulators which are a solder resist -- forming -- alternative -- opening -- carrying out -- a conductor -- [drawing 4 (l)] which exposes 5b and forms external terminal 7b. Then, external terminal 7a is formed. Other solder may be used although the PbSn (lead and tin) solder of 250 micrometers of diameters of a ball was used for external terminal 7a. Moreover, nothing may not be like external terminal 7b [drawing 4 (m)]. . At the end, it cuts and a semiconductor device 1 is obtained. Dicing equipment was used for cutting. Dicing conditions were set to the blade thickness of 50 micrometers, the cutting speed of 60mm/second, and rotational frequency 30000rpm [drawing 4 (n)].

[0018] Drawing 5 is the sectional view of the semiconductor device 1 of the 2nd example of this invention. the same reference number should give a part equivalent to the part of the example shown in drawing 1 in drawing 5 -- the explanation which overlaps in that of ********** is omitted. this example -- setting -- the conductor of the side face of a semiconductor device 1 -- external electrode 7c is prepared in 5b. Thereby, the further high density assembly becomes possible. Moreover, the manufacture approach of this semiconductor device 1 is the same as the manufacture approach of the semiconductor device 1 of drawing 1 , and after the cutting process shown in drawing 4 (n) is completed, it is acquired by laser's etc. removing 6d of some insulators, and preparing external electrode 7c.

[0019] As stated above, the description of the manufacture approach of the semiconductor device of this invention is that it can carry out wafer batch processing in spite of [drawing 3 (h)] cut once, in order to form wiring of a side face, after performing rewiring in the state of a wafer. Since the rewiring layer is supporting the semiconductor chip even if it cuts a wafer, positioning at each process is easy. Moreover, a man day can also be reduced for batch processing.

[0020] As mentioned above, although the desirable example of this invention was explained, proper modification is possible for this invention within limits which are not limited to these examples and do not deviate from the summary of this invention. For example, although a bump's formation approach was performed with electrolysis plating, you may form with the bonding method, vacuum deposition, or a replica method. moreover, the conductor same in the example -- although the external terminals 7b and 7c were formed on 5b, you may make it not form other external terminals in conductor 5b in which external terminal 7c was formed Moreover, in the example, all external terminals may prepare the external terminal mutually connected by Conductors 5a and 5b, without connecting with an electrode if

needed, although it connects with the electrode 3 of a semiconductor chip.

[Translation done.]